Features

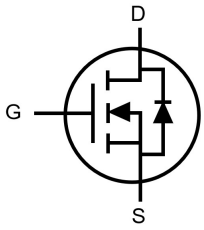
- SiC MOSFET technology
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Very low switching losses
- Low reverse recovery (Qrr)
- 100% Avalanche tested

Pb-Free RoHS HF Halogen-Free

V_{DS}	750	V
$R_{DS(on),TYP}$@ V_{GS}=15 V	25	mΩ
$I_{D(Silicon\ limited)}$	65	A

SOT-227

Part ID	Package Type	Marking	Packing
HCFZ030MR75KH0	SOT-227	030MR75KH0	12pcs/Tube



Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage		750	V
V_{GSmax}	Gate-Source voltage (dynamic) AC (f >1 Hz) ①		-8/+19	V
V_{GSop}	Gate-Source voltage (static) ②		-4/+15	V
I_D	Continuous drain current @VGS=15V (Silicon limited)	T_C = 25°C	65	A
I_D	Continuous drain current @VGS=15V (Silicon limited)	T_C = 100°C	46	A
I_{DM}	Pulse drain current tested,VGS=15V ③	T_C = 25°C	160	A
EAS	Maximum avalanche energy, single pulsed ④		1620	mJ
P_D	Maximum power dissipation ⑤	T_C = 25°C	205	W
		T_C = 100°C	103	W
T_{STG}	Storage temperature range		-55 to 150	°C
T_J	Operating junction temperature		-55 to 175	°C

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal resistance, junction-to-case ⑥	0.61	0.73	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient ⑦	18	22	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}=0V, I_D=250μA	750	--	--	V
I_{DSS}	Zero gate voltage drain current(Tj=25℃)	V_{DS}=750V,V_{GS}=0V	--	--	60	μA
	Zero gate voltage drain current(Tj=175℃)⑧	V_{DS}=750V,V_{GS}=0V	--	--	200	μA
I_{GSS}	Gate-body leakage current	V_{GS}=-4V,V_{DS}=0V	--	--	-200	nA
I_{GSS}	Gate-body leakage current	V_{GS}=15V,V_{DS}=0V	--	--	200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS},I_D=20mA	1.8	2.2	3.2	V
$R_{DS(on)}$	Drain-source on-state resistance ⑨	V_{GS}=15V, I_D=30A	--	25	30	mΩ
		Tj=175℃ ⑧	--	40	--	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
Ciss	Input capacitance ⑧	V_{DS}=400V,V_{GS}=0V, f=100KHz	--	2785	--	pF
Coss	Output capacitance ⑧		--	210	--	pF
Crss	Reverse transfer capacitance ⑧		--	15	--	pF
Rg	Gate resistance	f=1MHz	--	2.9	--	Ω
Qg	Total gate charge ⑧	V_{DS}=400V,I_D=30A, V_{GS}=-4/15V	--	99	--	nC
Qgs	Gate-source charge ⑧		--	17	--	nC
Qgd	Gate-drain charge ⑧		--	23	--	nC
Switching Characteristics ⑧						
Td(on)	Turn-on delay time	V_{DD}=400V, I_D=30A, R_G=12Ω, V_{GS}=-4/15V L=1.5mH (Fig17)	--	34	--	ns
Tr	Turn-on rise time		--	124	--	ns
Td(off)	Turn-off delay time		--	83	--	ns
Tf	Turn-off fall time		--	136	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=30A,V_{GS}=-4V	--	4.2	6	V
Trr	Reverse recovery time ⑧	V_{DD}=100V I_{sd}=30A, V_{GS}=0V di/dt=500A/μs	--	21	--	ns
Qrr	Reverse recovery charge ⑧		--	62	--	nC
Irrm	Peak Reverse Recovery Current ⑧		--	5.2	--	A

NOTE:

① When using MOSFET Body Diode VGSmax = -8V/+19V

② MOSFET can also safely operate at -4/+15 V

③ Single pulse; pulse width limited by max junction temperature.

④ This maximum value is based on starting T_J = 25°C, L = 10mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} =15V； 100% FT tested at L = 10mH, I_{AS} = 16A.

⑤ The power dissipation Pd is based on Tj(max), using junction-to-case thermal resistance RθJC.

⑥ Thermal resistance from junction to soldering point (on the exposed drain pad). These tests are performed on a cool plate.

⑦ The value of RθJA is measured with the device in a still air environment with TA =25°C.

⑧ Guaranteed by design, not subject to production testing.

⑨ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

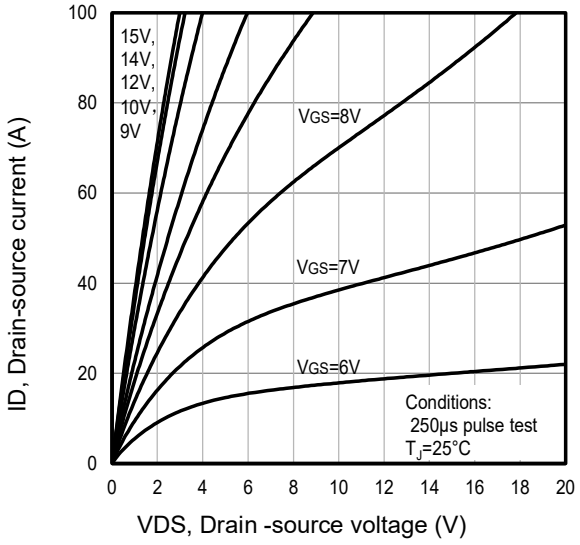


Fig1. Typical output characteristics

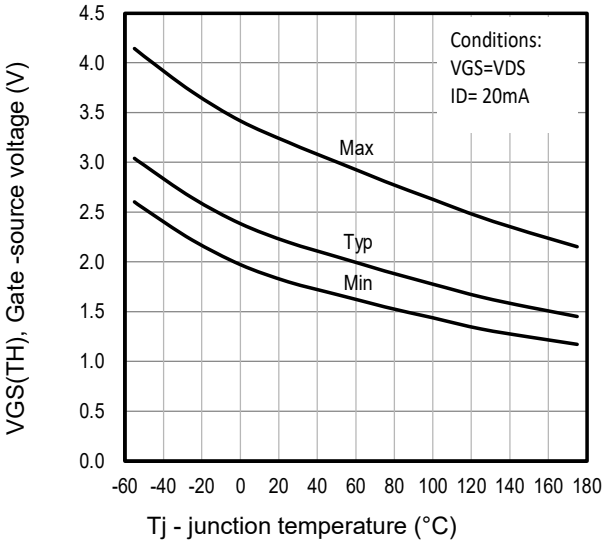


Fig2. Typical $V_{GS(TH)}$ gate -source voltage Vs. Tj

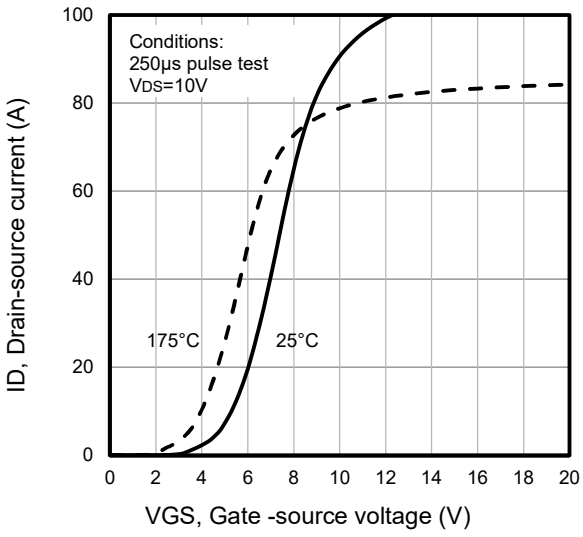


Fig3. Typical transfer characteristics

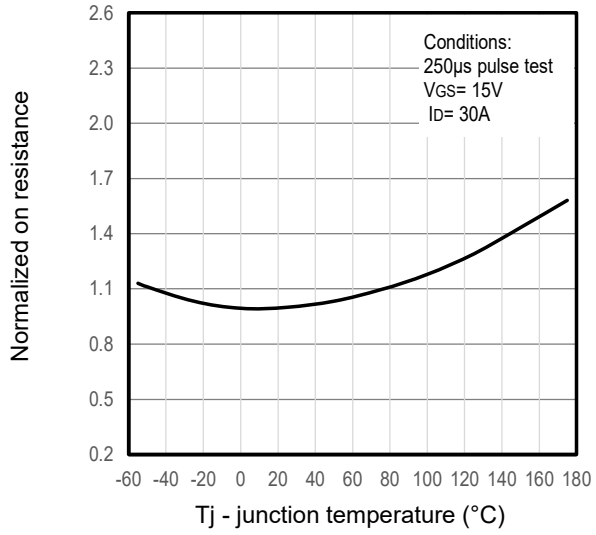


Fig4. Typical normalized on-resistance Vs. Tj

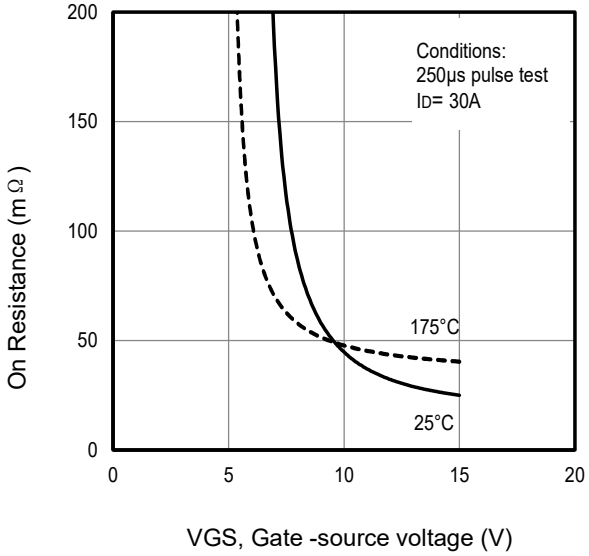


Fig5. Typical on resistance Vs gate -source voltage

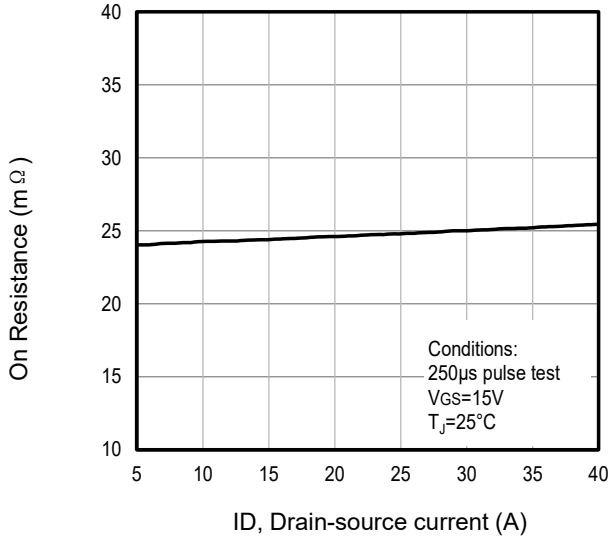


Fig6. Typical on resistance Vs drain current

Typical Characteristics

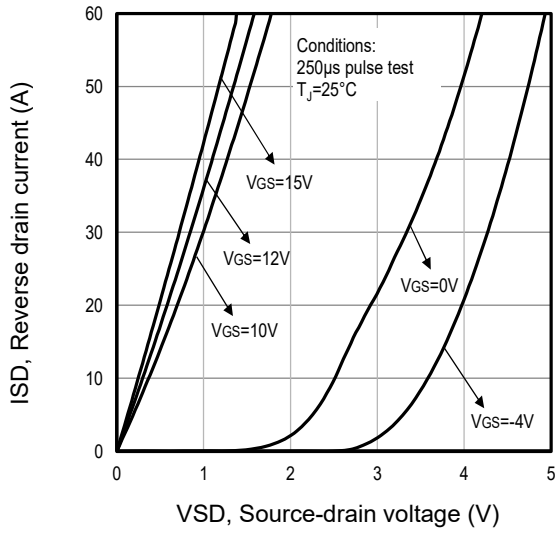


Fig7. Typical source-drain diode forward voltage

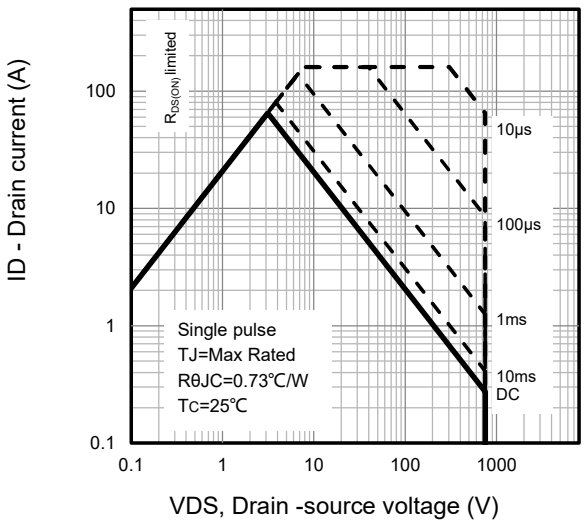


Fig8. Maximum safe operating area

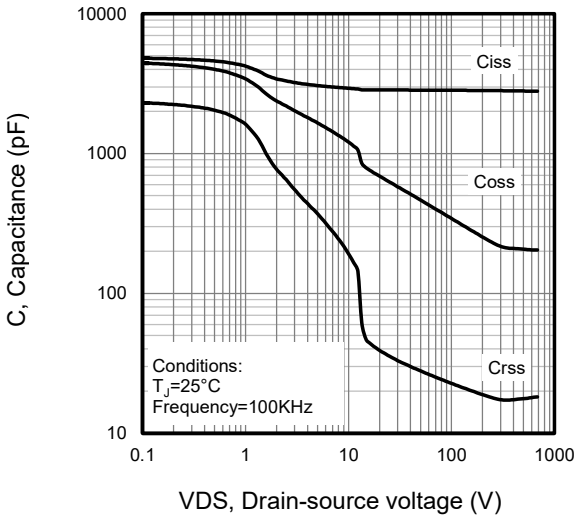


Fig9. Typical capacitance Vs. drain-source voltage

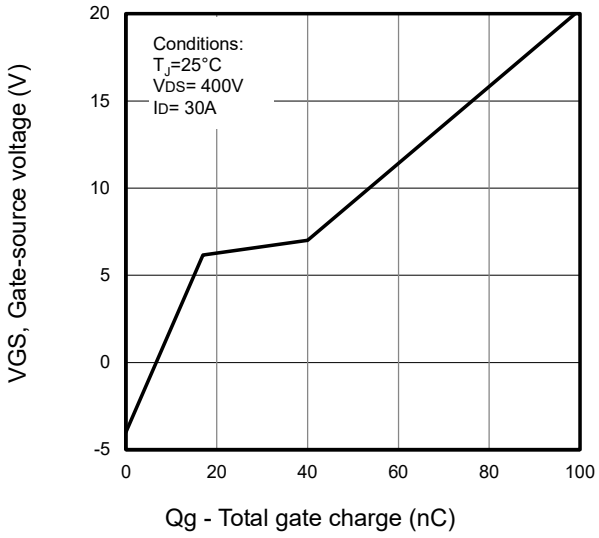


Fig10. Typical gate charge Vs. gate-source voltage

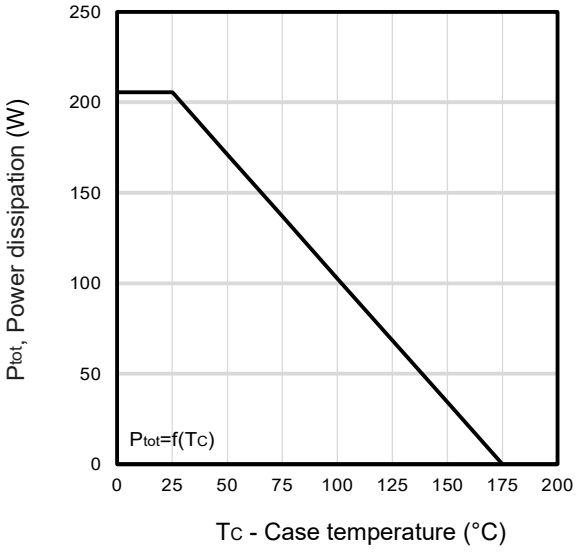


Fig11. Power dissipation Vs. case temperature

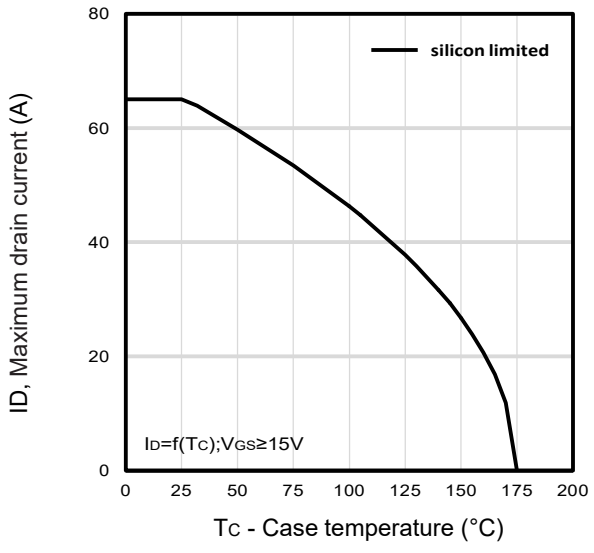


Fig12. Maximum drain current Vs. case temperature

Typical Characteristics

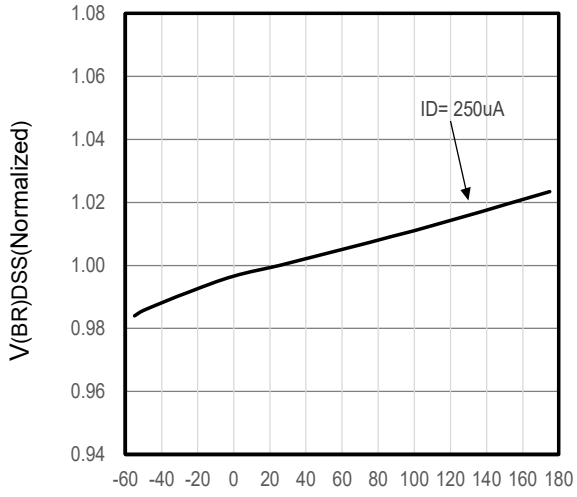


Fig13. Typical $V_{(BR)DSS}$ Vs Tj

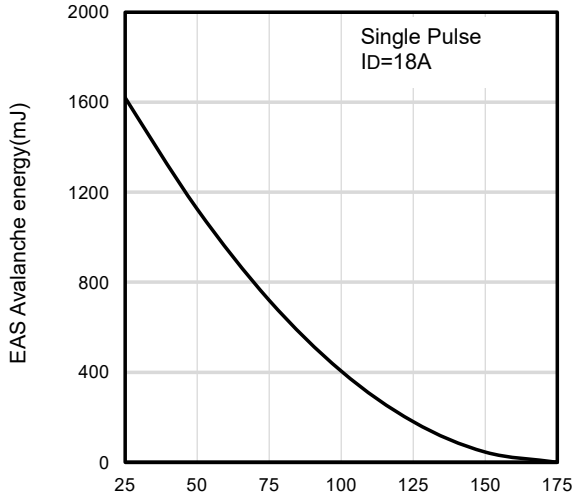


Fig14. Maximum avalanche energy vs temperature (°C)

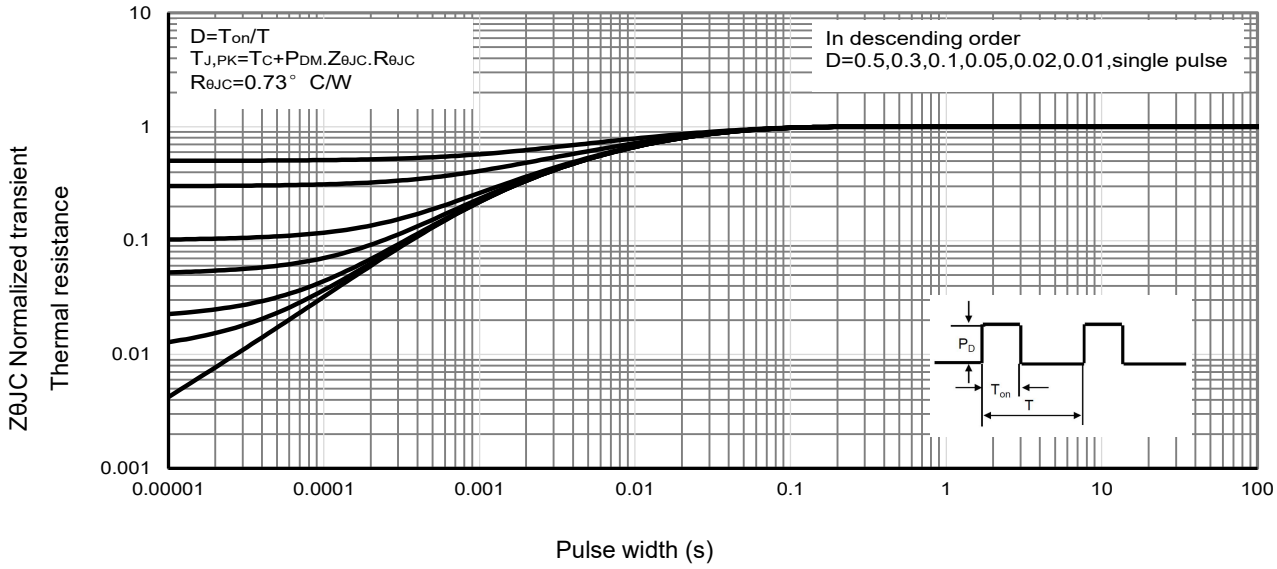


Fig15 . Normalized maximum transient thermal impedance

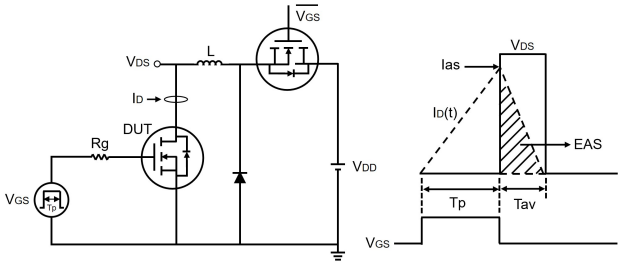


Fig16. Unclamped inductive test circuit and waveforms

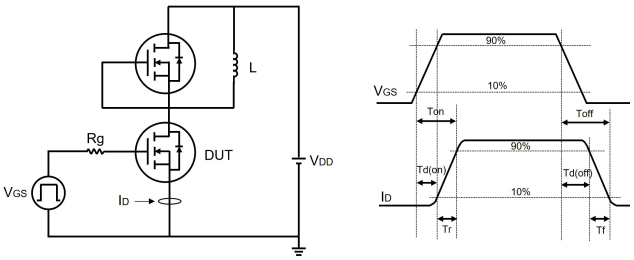
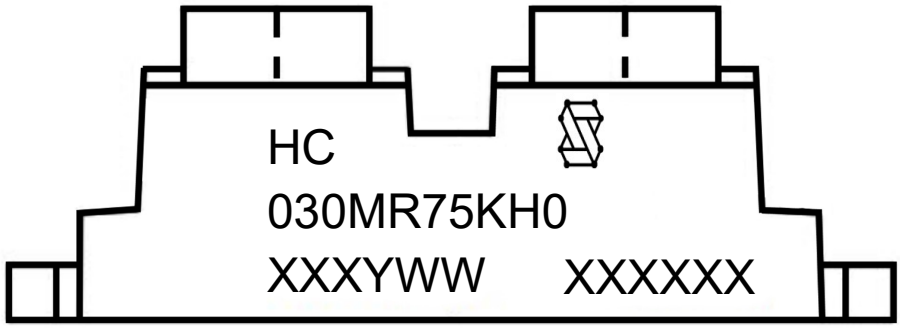


Fig17. Switching Energy Measurement Circuit

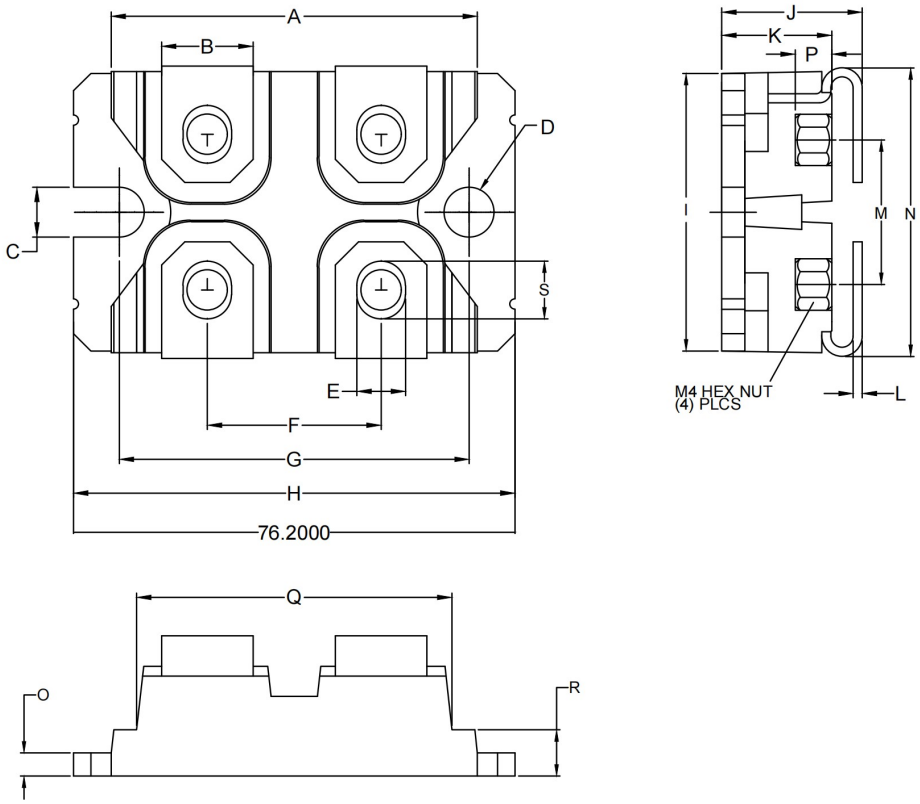
Marking Information



1st line: Vergiga Code（HC）， Vergiga Logo
2nd line: Part Number（030MR75KH0）
3rd line: Date code （XXXYWW）
XXX: Wafer lot number code , code changed with lot number
Y: Year code ， refer to table below
WW: Week code (01 to 53)
XXXXXX: Modules serial number code

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

SOT-227 Package Outline Data



Symbol	Dimensions (unit: mm)		Symbol	Dimensions (unit: mm)	
	Min	Max		Min	Max
A	31.40	31.60	K	9.40	9.60
B	7.70	8.10	L	0.75	0.85
C	4.20	4.40	M	12.40	12.60
D	4.20	4.40	N	24.50	25.40
E	4.10	4.30	O	1.90	2.10
F	14.90	15.10	P	3.10	3.20
G	30.10	30.20	Q	26.60	27.00
H	38.00	38.40	R	3.80	4.20
I	23.80	24.20	S	5.10	5.40
J	12.20	12.70	/	/	/